

ABSTRACT OF THE DISCLOSURE

A flash memory structure which includes a tunneling oxide layer, a floating gate, a dielectric stacked layer, a control gate and a source/drain region. The dielectric stacked layer is formed by successively stacking a first oxide layer, a dielectric layer made of a high dielectric constant material and a second oxide layer, and is installed between the floating gate and the control gate. The floating gate is formed on the tunneling oxide layer. The control gate is formed on the dielectric stacked layer. The source/drain region is installed within the substrate on the two sides of the floating gate.

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